CLAIMS

1. A phase locked loop (PLL) circuit comprising:

a phase comparator that receives a reference clock signal and a comparison clock signal, compares a phase of the reference clock signal with a phase of the comparison clock signal, produces a rectangular wave signal having three voltage levels corresponding to phase differences, and outputs the rectangular wave signal;

a level shifter that receives the rectangular wave signal outputted from the phase comparator, shifts a voltage level of the rectangular wave signal, and outputs the rectangular wave signal whose voltage level has been shifted;

a voltage controlled oscillator (VCO) that receives the rectangular wave signal outputted from the level shifter, and outputs a clock signal whose frequency corresponds to the voltage level of the rectangular wave signal; and

a frequency divider that divides the frequency of the clock signal outputted from the VCO by N (N is a counting number), and feeds back a signal whose frequency is divided to the phase comparator as the comparison clock signal.

2. The PLL circuit of claim 1, wherein the phase comparator compares the phase of the reference clock signal with the phase of the comparison clock signal on every cycle of the reference clock signal, and produces the rectangular wave signal having three levels, a high voltage level, a low

voltage level, and a reference level.

3. PLL circuit of claim 2, wherein the phase comparator produces a rectangular wave signal having a high voltage level by making duration of the rectangular wave signal having the high voltage level proportional to a phase difference when the comparison clock signal has the phase difference caused by a phase lag, and produces a rectangular wave signal having a low voltage level by making duration of the rectangular wave signal having the low voltage level proportional to the phase difference when the comparison clock signal has the phase difference caused by a phase lead, and outputs a reference level signal without outputting the rectangular wave signal having the high or low voltage level when there is no phase difference.

4. The PLL circuit of claim 1, wherein the level shifter converts three voltage levels, a voltage level of the rectangular wave signal having the high voltage level, a voltage level of the rectangular wave signal having the low voltage level, and a voltage level of the reference level, to a voltage level for controlling a VCO.

5. The PLL circuit of claim 4, wherein the level shifter includes:

a plurality of resistors connected in series; and

a switch that produces the voltage level for controlling a VCO by switching connections of the plurality of resistors based on the three voltage levels.

6. The PLL circuit of claim 1, wherein the phase comparator compares the phase of the reference clock signal with the phase of the comparison clock signal on every cycle of the reference clock signal, and produces the rectangular wave signal having three levels, a high voltage level, a low voltage level, and a reference level.

7. The PLL circuit of claim 1, wherein the VCO has an arbitrary voltage-frequency characteristic.

8. The PLL circuit of claim 1, wherein a mathematical model is used as a principle of operation of the PLL circuit, the mathematical model expressing a response from the PLL circuit by a numeric sequence.

9. A phase synchronization method for a phase locked loop (PLL) circuit comprising:

receiving a reference clock signal and a comparison clock signal, comparing a phase of the reference clock signal with a phase of the comparison clock signal, producing a rectangular wave signal having three voltage levels corresponding to phase differences, and outputting the rectangular wave signal;

receiving the rectangular wave signal, shifting a voltage level of the rectangular wave signal, and outputting the rectangular wave signal whose voltage level has been shifted;

receiving the rectangular wave signal whose voltage level has been shifted, and outputting a clock signal whose frequency corresponds to the

voltage level of the rectangular wave signal; and

dividing the frequency of the clock signal by N (N is a counting number), and feeding back a signal whose frequency is divided to the phase comparator as the comparison clock signal.

10. The phase synchronization method for a PLL circuit of claim 9, wherein the comparing the phases of the signals includes comparing the phases on every cycle of the reference clock signal, and the producing the rectangular wave signal includes producing the rectangular wave signal having three levels, a high voltage level, a low voltage level, and a reference level.

11. An operation analysis method for a phase locked loop (PLL) circuit, the PLL circuit including:

a phase comparator that receives a reference clock signal and a comparison clock signal, compares a phase of the reference clock signal with a phase of the comparison clock signal, produces a rectangular wave signal having a predetermined voltage level, duration of which corresponds to a phase difference, and outputs the rectangular wave signal;

a voltage controlled oscillator (VCO) that receives a signal outputted from the phase comparator, and outputs a clock signal whose frequency corresponds to a voltage level of the signal; and

a frequency divider that divides the frequency of the clock signal outputted from the VCO by N (N is a counting number), and feeds back a signal whose frequency is divided to the phase comparator as the

comparison clock signal,

the operation analysis method comprising:

analyzing an operation for the phase difference between the reference clock signal and the compression clock signal by using a mathematical model expressed below:

$\theta_n=(1-((G\cdot T)/(2\pi\cdot N)))^n\cdot\theta$

n: a counting number

π: a circle ratio

G: a fixed number corresponding to the voltage-frequency characteristic of the VCO

T: an oscillation cycle of the reference clock signal

N: a frequency divisor (a counting number) of the frequency divider

θ: a phase difference at time 0

θ_n: a phase difference at time nT